FIG.1

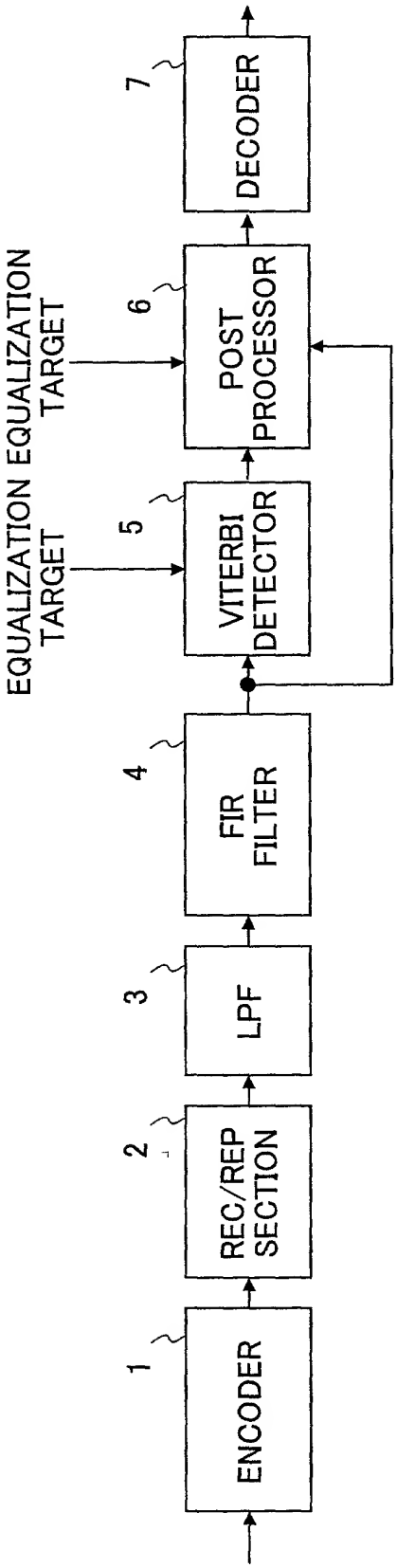

ENCODER
1
REC/REP SECTION
2
LPF
3
FIR FILTER
4
EQUALIZATION TARGET
VITERBI DETECTOR
5
EQUALIZATION TARGET
POST PROCESSOR
6
DECODER
7

FIG. 2

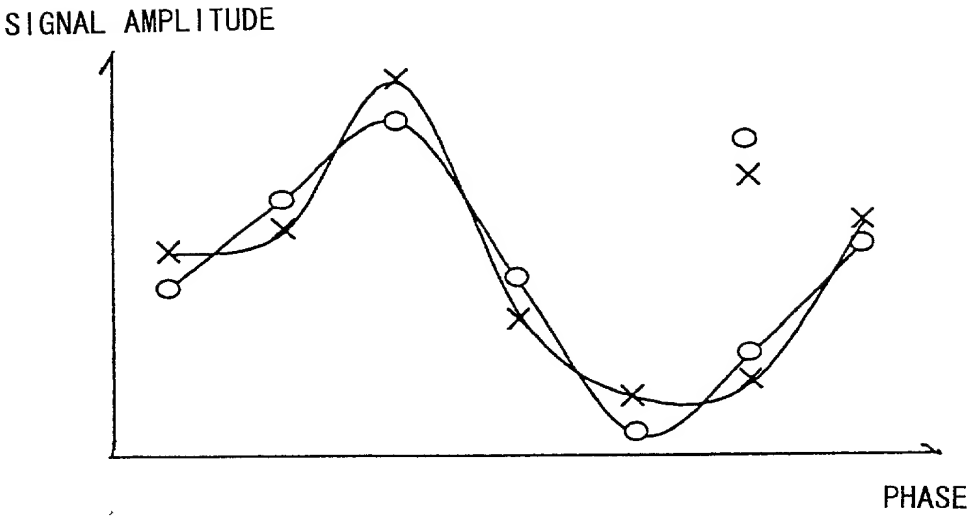


FIG.3

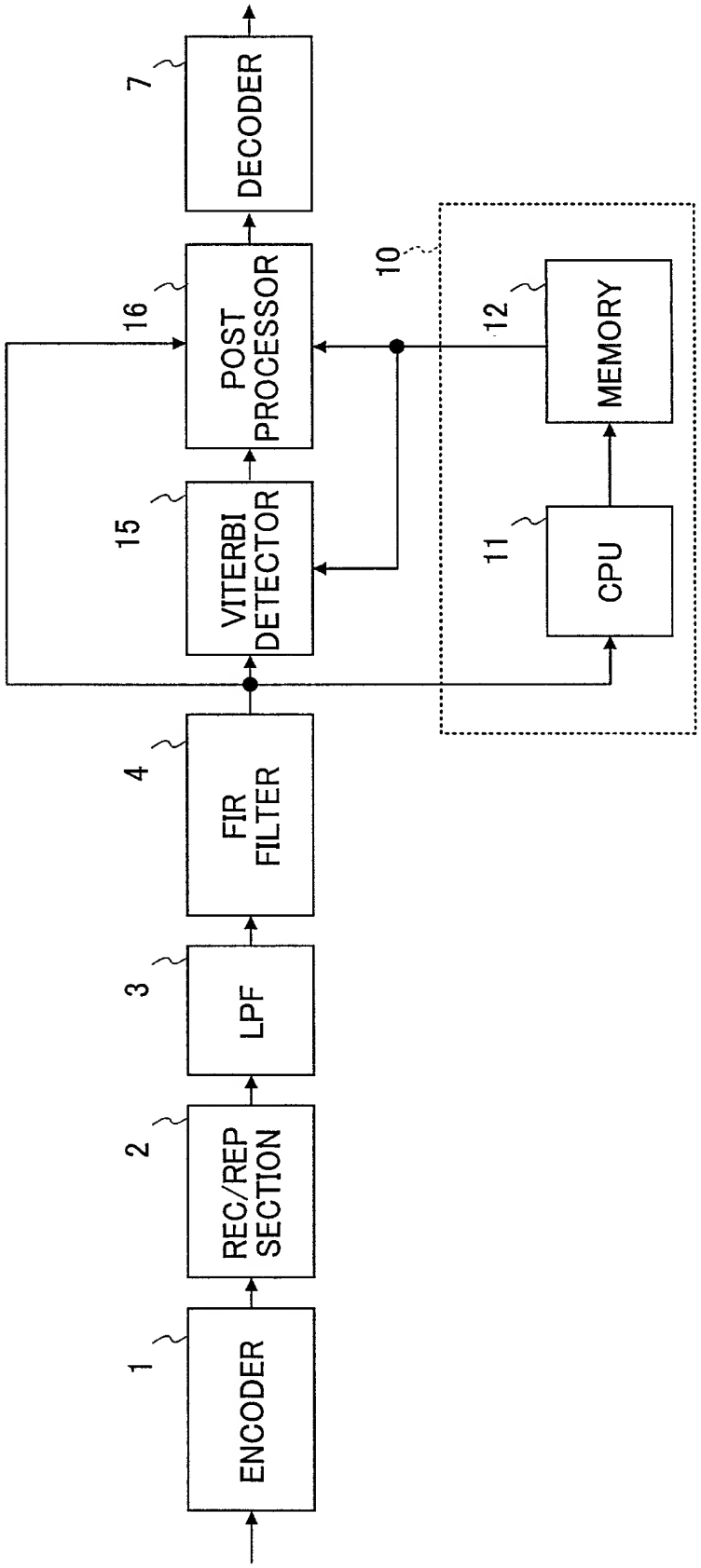

ENCODER
1
REC/REP SECTION
2
LPF
3
FIR FILTER
4
VITERBI DETECTOR
15
POST PROCESSOR
16
DECODER
7
10
CPU
11
MEMORY
12

FIG.4

$a_{k-3}a_{k-2}a_{k-1}a_k$	EQUALIZATION OUTPUT b_K	
	IDEAL EQUALIZATION VALUE	AVERAGE VALUE OF ACTUAL EQUALIZED WAVEFORM
0000	0	μ_0
0001	+1	μ_1
0010	+1	μ_2
0011	+2	μ_3
0100	−1	μ_4
0101	0	μ_5
0110	0	μ_6
0111	+1	μ_7
1000	−1	μ_8
1001	0	μ_9
1010	0	μ_{10}
1011	+1	μ_{11}
1100	−2	μ_{12}
1101	−1	μ_{13}
1110	−1	μ_{14}
1111	0	μ_{15}

FIG.5

$a_{k-2}a_{k-1}a_k$	STATE
000	S_0
001	S_1
010	S_2
011	S_3
100	S_4
101	S_5
110	S_6
111	S_7

MAGNETIC RECORDING AND/OR REPRODUCING . . .
Ichihara et al.
Greer, Burns & Crain, Ltd. (James K. Folker)
Ref. No. 0941.65729
Sheet 6 of 25 (312) 360 0080

FIG.6

STATE OF 1 BIT BEFORE	PRESENT STATE			PRESENT EQUALIZATION OUTPUT b_k					
				IDEAL VALUE			AVERAGE VALUE OF ACTUAL EQUALIZED WAVEFORM		
	a_k	0	1	a_k	0	1	a_k	0	1
S_0		S_0	S_1		0	+1		μ_0	μ_1
S_1		S_2	S_3		+1	+2		μ_2	μ_3
S_2		S_4	S_5		−1	0		μ_4	μ_5
S_3		S_6	S_7		0	+1		μ_6	μ_7
S_4		S_0	S_1		−1	0		μ_8	μ_9
S_5		S_2	S_3		0	+1		μ_{10}	μ_{11}
S_6		S_4	S_5		−2	−1		μ_{12}	μ_{13}
S_7		S_6	S_7		−1	0		μ_{14}	μ_{15}

FIG. 7

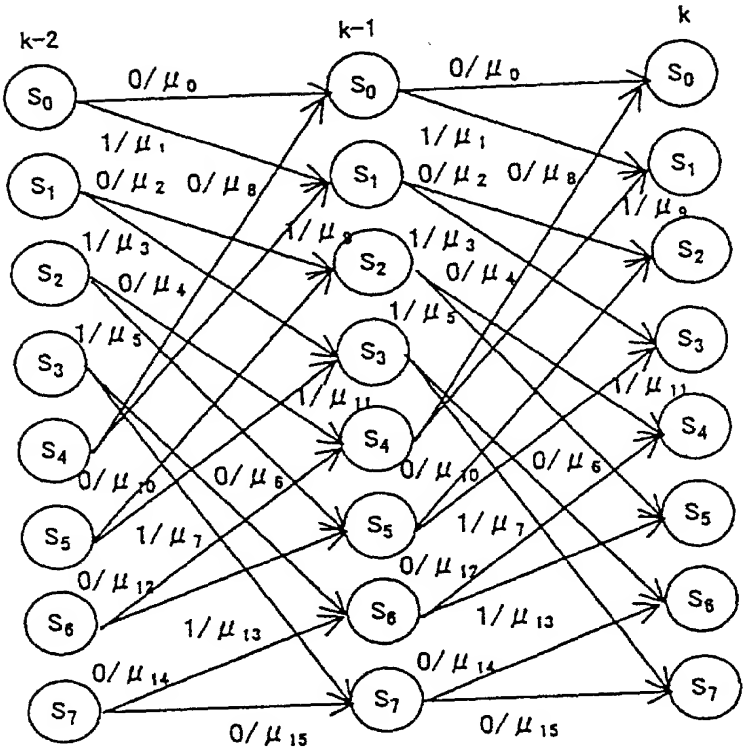

k-2
k-1
k
S0
S1
S2
S3
S4
S5
S6
S7
0/μ0
1/μ1
0/μ2
0/μ8
1/μ9
1/μ3
0/μ4
1/μ5
1/μ11
0/μ10
0/μ6
1/μ7
0/μ12
1/μ13
0/μ14
0/μ15

FIG. 8

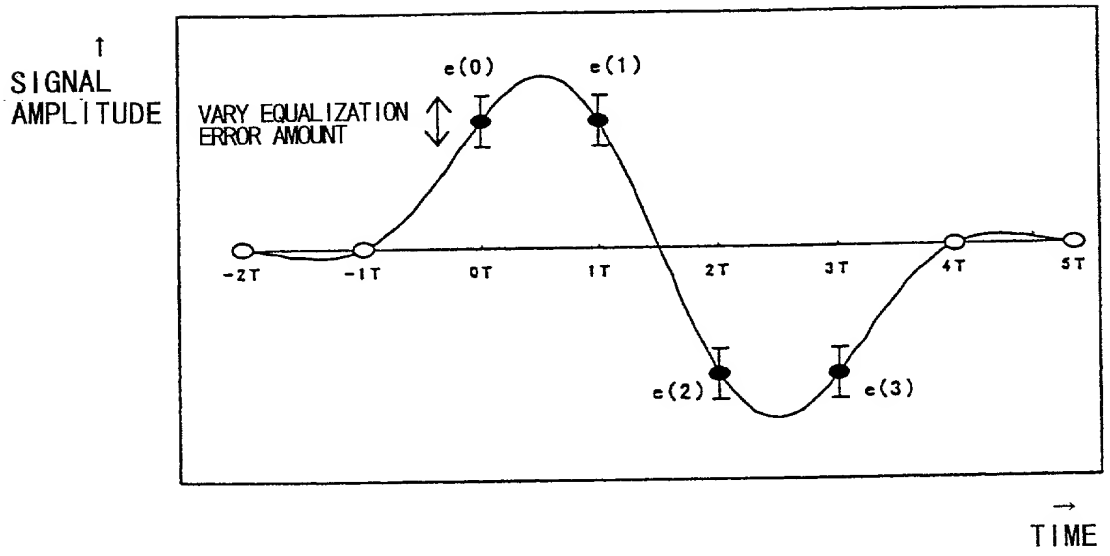

SIGNAL AMPLITUDE
VARY EQUALIZATION ERROR AMOUNT
e(0)
e(1)
e(2)
e(3)
-2T
-1T
0T
1T
2T
3T
4T
5T
TIME

FIG. 9

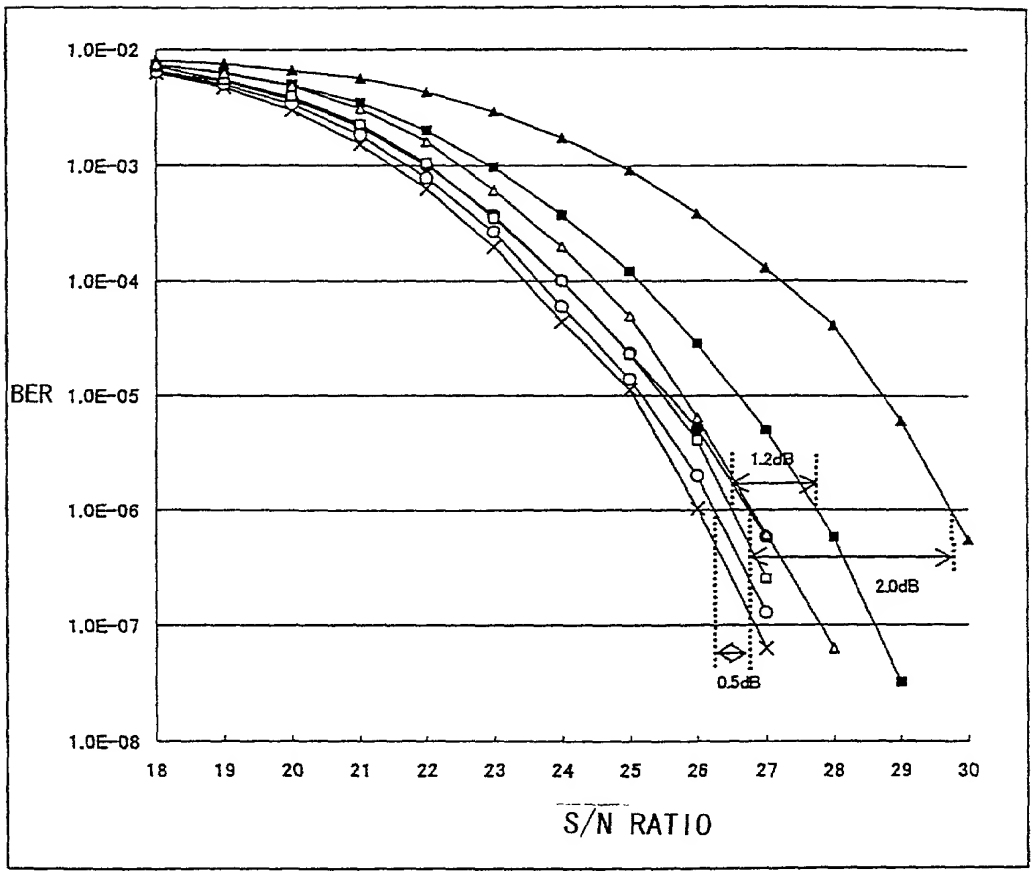

1.0E-02
1.0E-03
1.0E-04
BER 1.0E-05
1.0E-06
1.0E-07
1.0E-08
18
19
20
21
22
23
24
25
26
27
28
29
30
S/N RATIO
1.2dB
2.0dB
0.5dB

FIG.10

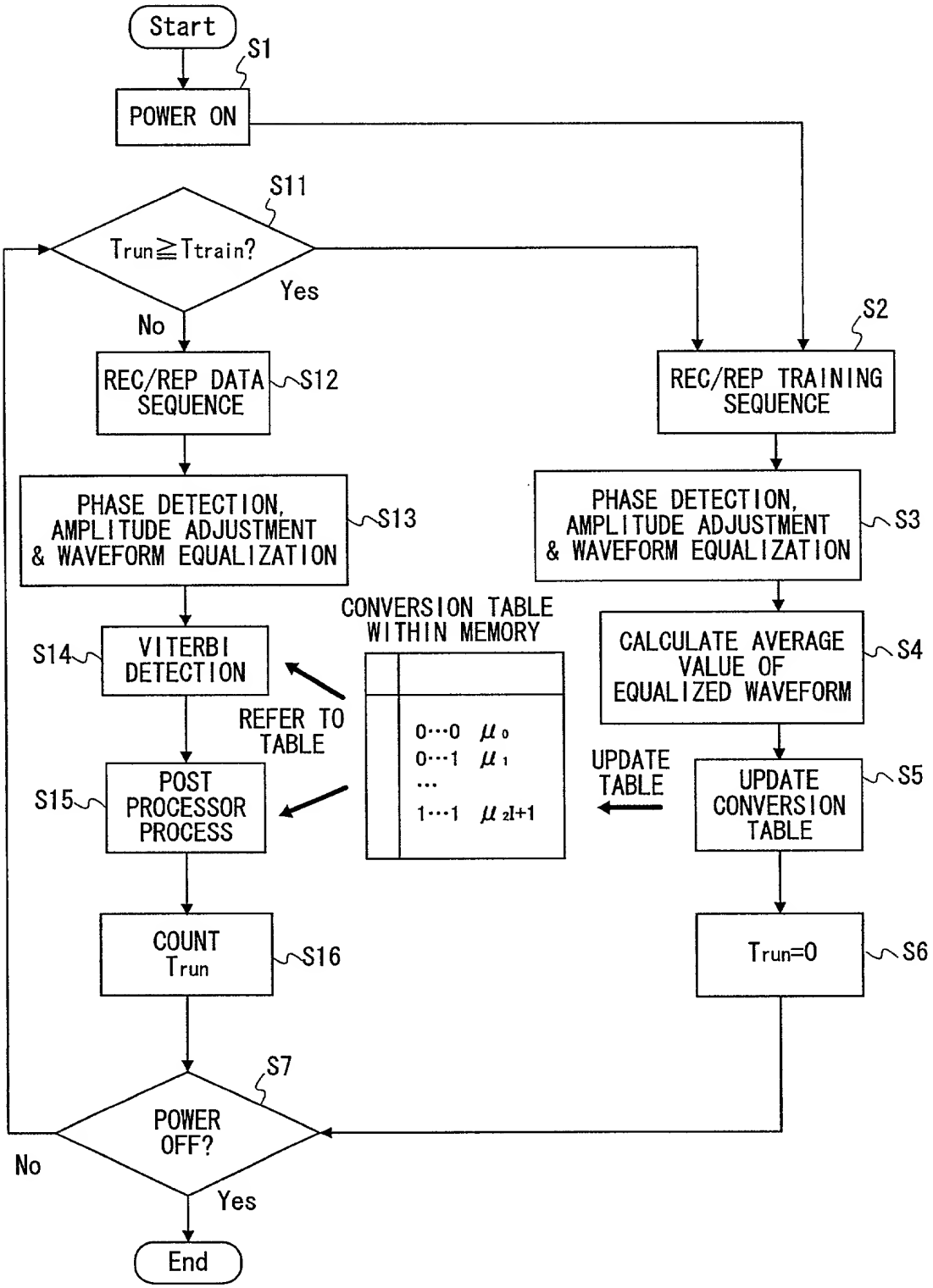

Start
S1
POWER ON
S11
Trun≧Ttrain?
Yes
No
REC/REP DATA SEQUENCE
S12
S2
REC/REP TRAINING SEQUENCE
PHASE DETECTION, AMPLITUDE ADJUSTMENT & WAVEFORM EQUALIZATION
S13
PHASE DETECTION, AMPLITUDE ADJUSTMENT & WAVEFORM EQUALIZATION
S3
CONVERSION TABLE WITHIN MEMORY
S14
VITERBI DETECTION
REFER TO TABLE
0…0 μ0
0…1 μ1
…
1…1 μ2I+1
CALCULATE AVERAGE VALUE OF EQUALIZED WAVEFORM
S4
UPDATE TABLE
S15
POST PROCESSOR PROCESS
UPDATE CONVERSION TABLE
S5
COUNT Trun
S16
Trun=0
S6
S7
POWER OFF?
No
Yes
End

FIG.11

a_{k-2}	a_{k-1}	a_k	COMPENSATION AMOUNT
0	0	1	–
0	1	1	T_{01}
1	0	1	T_{10}
1	1	1	T_{11}

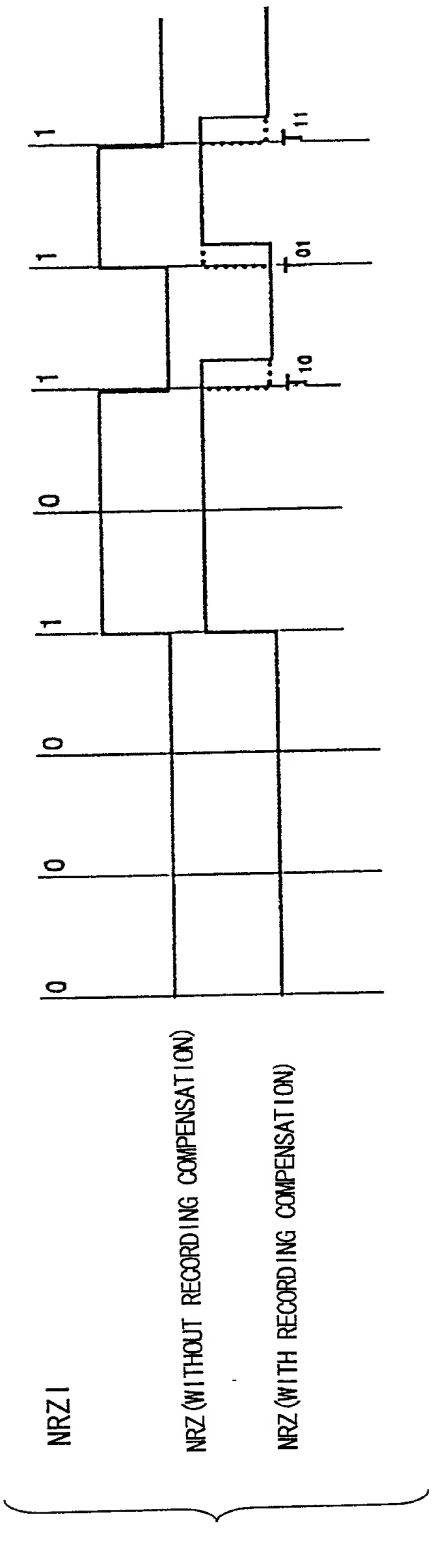
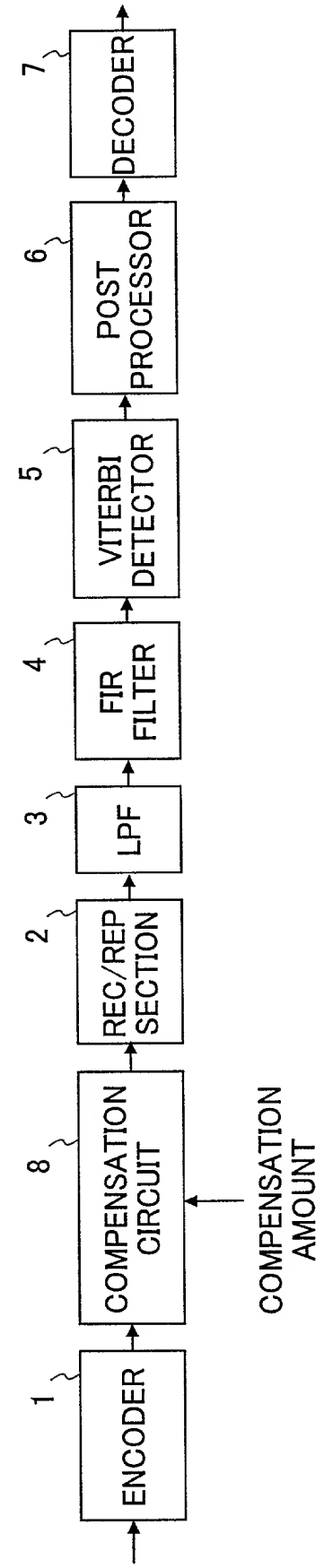

1
1
1
0
1
0
0
0
11
01
10
NRZI
NRZ (WITHOUT RECORDING COMPENSATION)
NRZ (WITH RECORDING COMPENSATION)

FIG. 12

FIG.13


ENCODER
1
COMPENSATION CIRCUIT
8
COMPENSATION AMOUNT
REC/REP SECTION
2
LPF
3
FIR FILTER
4
VITERBI DETECTOR
5
POST PROCESSOR
6
DECODER
7

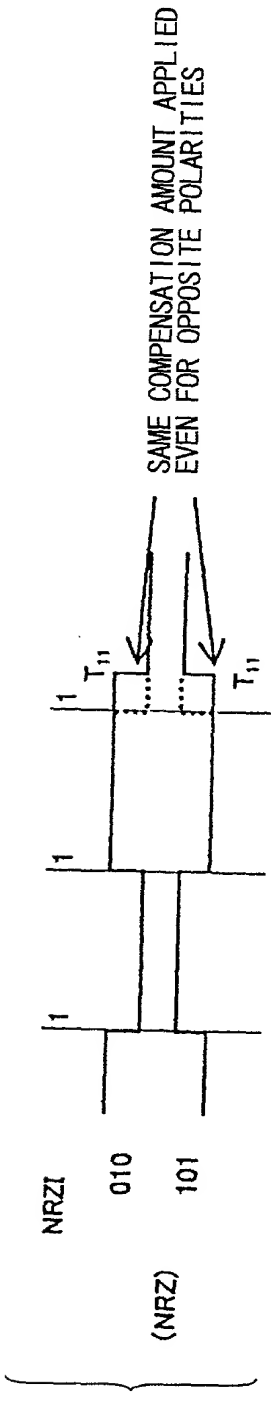

SAME COMPENSATION AMOUNT APPLIED EVEN FOR OPPOSITE POLARITIES
T_{11}
T_{11}
1
1
1
NRZI
010
101
(NRZ)

FIG. 14

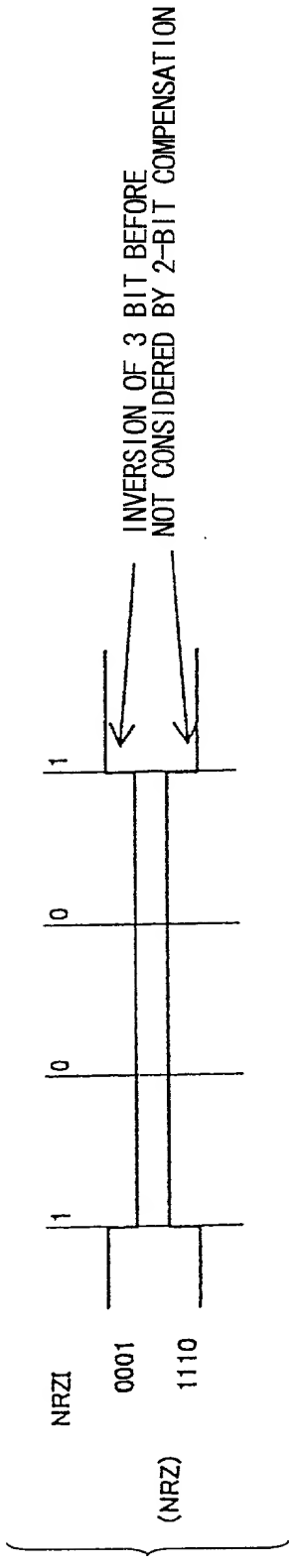

INVERSION OF 3 BIT BEFORE
NOT CONSIDERED BY 2-BIT COMPENSATION
1
0
0
1
NRZI
0001
1110
(NRZ)

FIG. 15

FIG.16

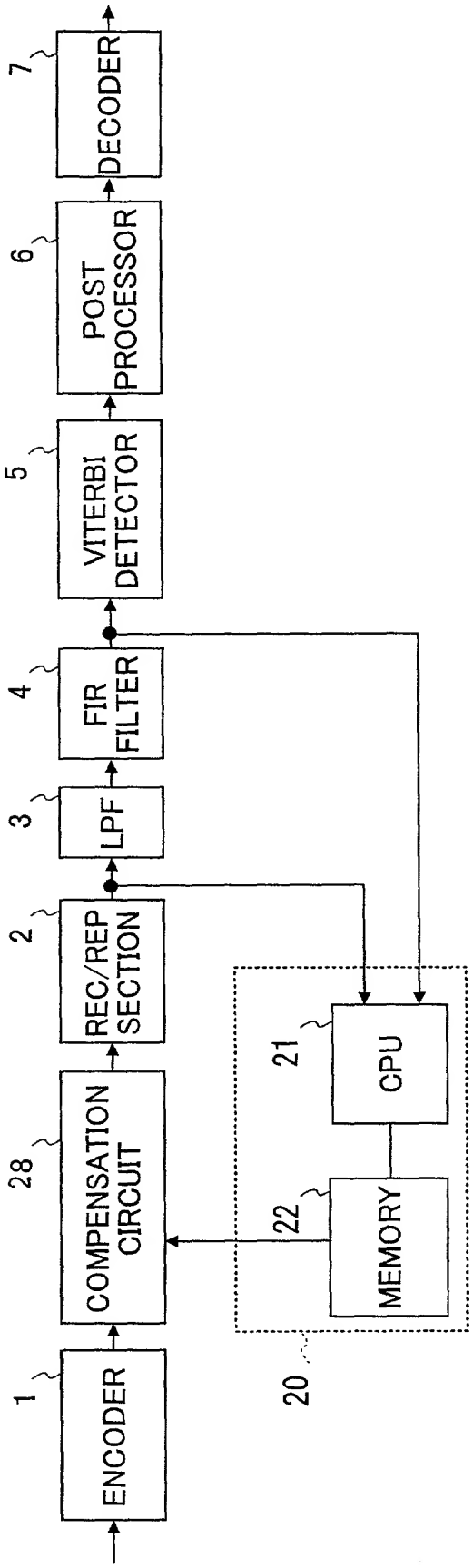

ENCODER
1
COMPENSATION CIRCUIT
28
REC/REP SECTION
2
LPF
3
FIR FILTER
4
VITERBI DETECTOR
5
POST PROCESSOR
6
DECODER
7
CPU
21
MEMORY
22
20

FIG.17

a_{k-1}	. . .	a_k	. . .	a_{k+1}	POLARITY	COMPENSATION AMOUNT
0	. . .	1	. . .	0	+	$T_{0\cdots1\cdots0+}$
					−	$T_{0\cdots1\cdots0-}$
. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	. . .	1	. . .	1	+	$T_{0\cdots1\cdots1+}$
					−	$T_{0\cdots1\cdots1-}$

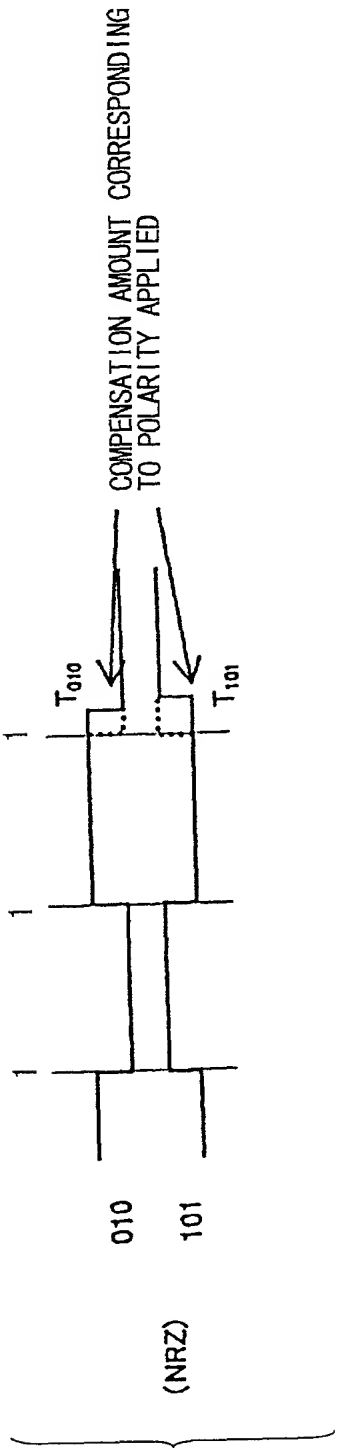

COMPENSATION AMOUNT CORRESPONDING TO POLARITY APPLIED
T_{010}
T_{101}
1
1
1
010
101
(NRZ)

FIG. 18

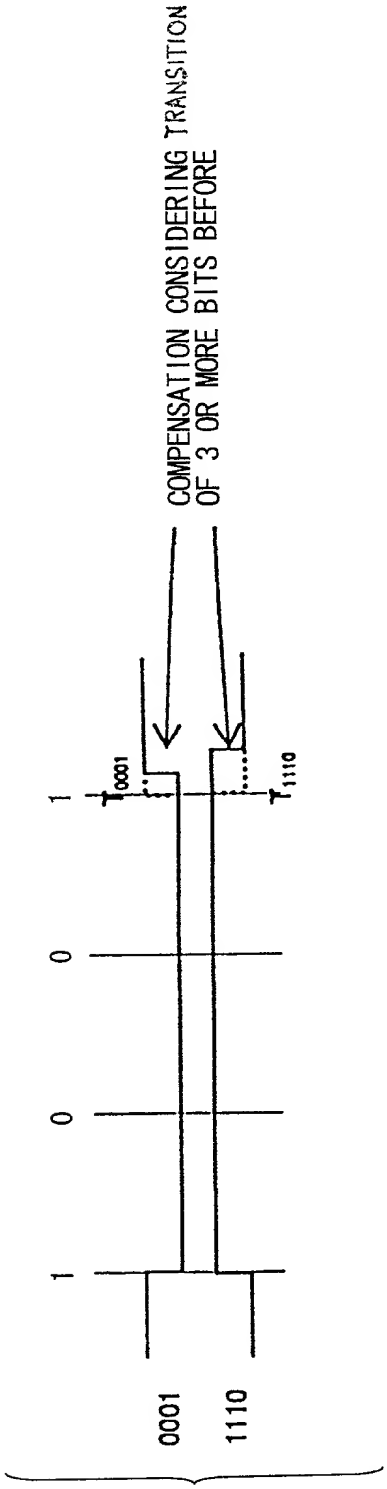

COMPENSATION CONSIDERING TRANSITION
OF 3 OR MORE BITS BEFORE
T0001
T1110
1
0
0
1
0001
1110

FIG. 19

FIG.20

RECORDING SEQUENCE					AVERAGE VALUE w(t) ($-1 \leqq t \leqq 1$) OF OVER-SAMPLED REPRODUCED OR EQUALIZED WAVEFORM							
a_{k-1}	···	a_k	···	a_{k+1}	POLARITY	w(−1)	···	w(0)	···	w(1)	···
0	···	1	···	0	+	$W(-1)_{0\cdots1\cdots0+}$	···	$W(0)_{0\cdots1\cdots0+}$	···	$W(1)_{0\cdots1\cdots0+}$	···
					−	$W(-1)_{0\cdots1\cdots0-}$	···	$W(0)_{0\cdots1\cdots0-}$	···	$W(1)_{0\cdots1\cdots0-}$	···
0	···	1	···	0	+	$W(-1)_{0\cdots1\cdots1+}$	···	$W(0)_{0\cdots1\cdots1+}$	···	$W(1)_{0\cdots1\cdots1+}$	···
					−	$W(-1)_{0\cdots1\cdots1-}$	···	$W(0)_{0\cdots1\cdots1-}$	···	$W(1)_{0\cdots1\cdots1-}$	···
···	···	···	···	···	···	···	···	···	···	···	···
1	···	1	···	0	+	$W(-1)_{1\cdots1\cdots0+}$	···	$W(0)_{1\cdots1\cdots0+}$	···	$W(1)_{1\cdots1\cdots0+}$	···
					−	$W(-1)_{1\cdots1\cdots0-}$	···	$W(0)_{1\cdots1\cdots0-}$	···	$W(1)_{1\cdots1\cdots0-}$	···
1	···	1	···	1	+	$W(-1)_{1\cdots1\cdots1+}$	···	$W(0)_{1\cdots1\cdots1+}$	···	$W(1)_{1\cdots1\cdots1+}$	···
					−	$W(-1)_{1\cdots1\cdots1-}$	···	$W(0)_{1\cdots1\cdots1-}$	···	$W(1)_{1\cdots1\cdots1-}$	···

MAGNETIC RECORDING AND/OR REPRODUCING . . .
Ichihara et al.
Greer, Burns & Crain, Ltd. (James K. Folker)
Ref. No. 0941.65729
Sheet 20 of 25 (312) 360 0080

FIG. 21

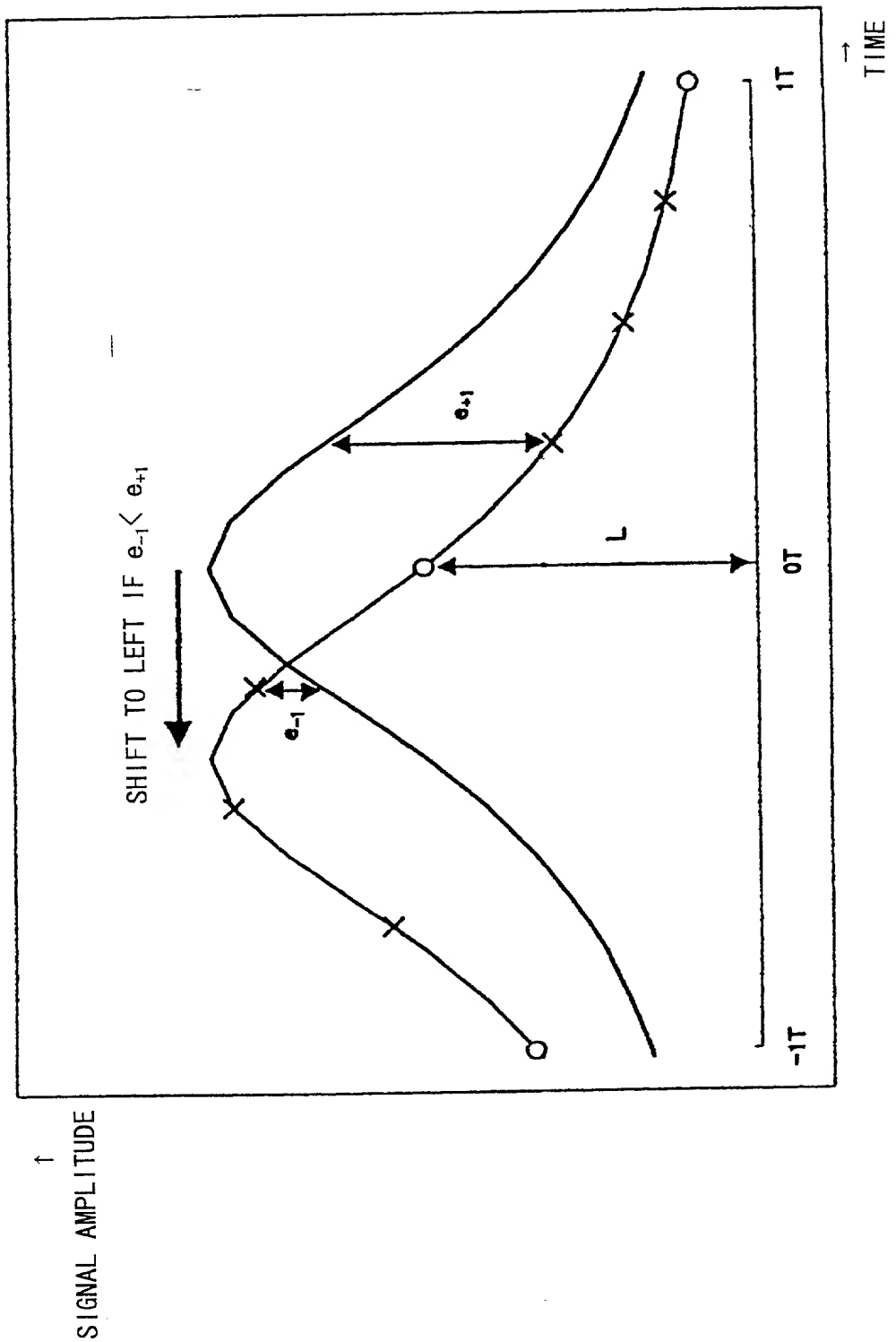


FIG. 22

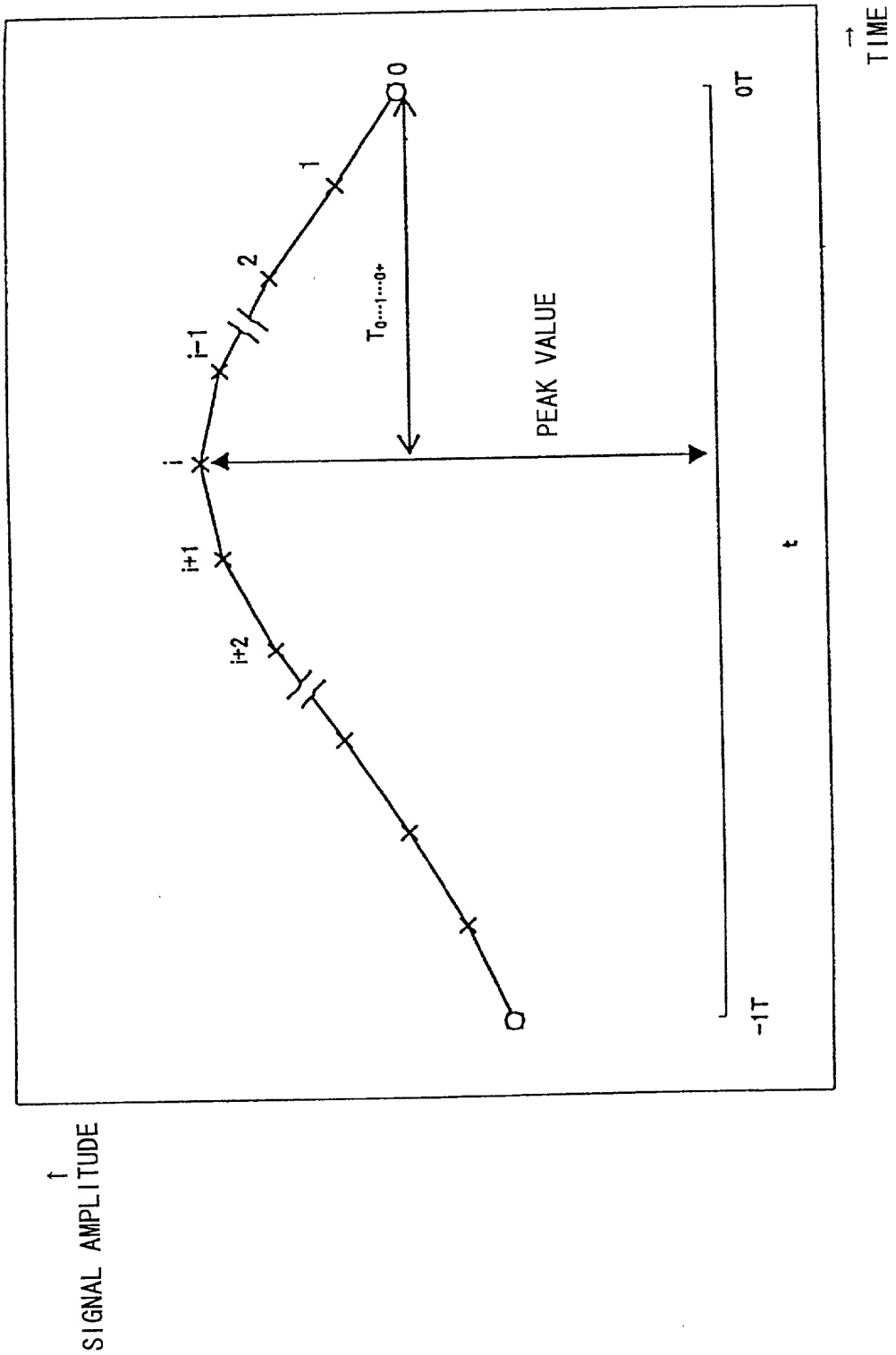

SIGNAL AMPLITUDE
TIME
0T
-1T
t
0
1
2
i-1
i
i+1
i+2
$T_{0\cdots1\cdots0+}$
PEAK VALUE

FIG. 23

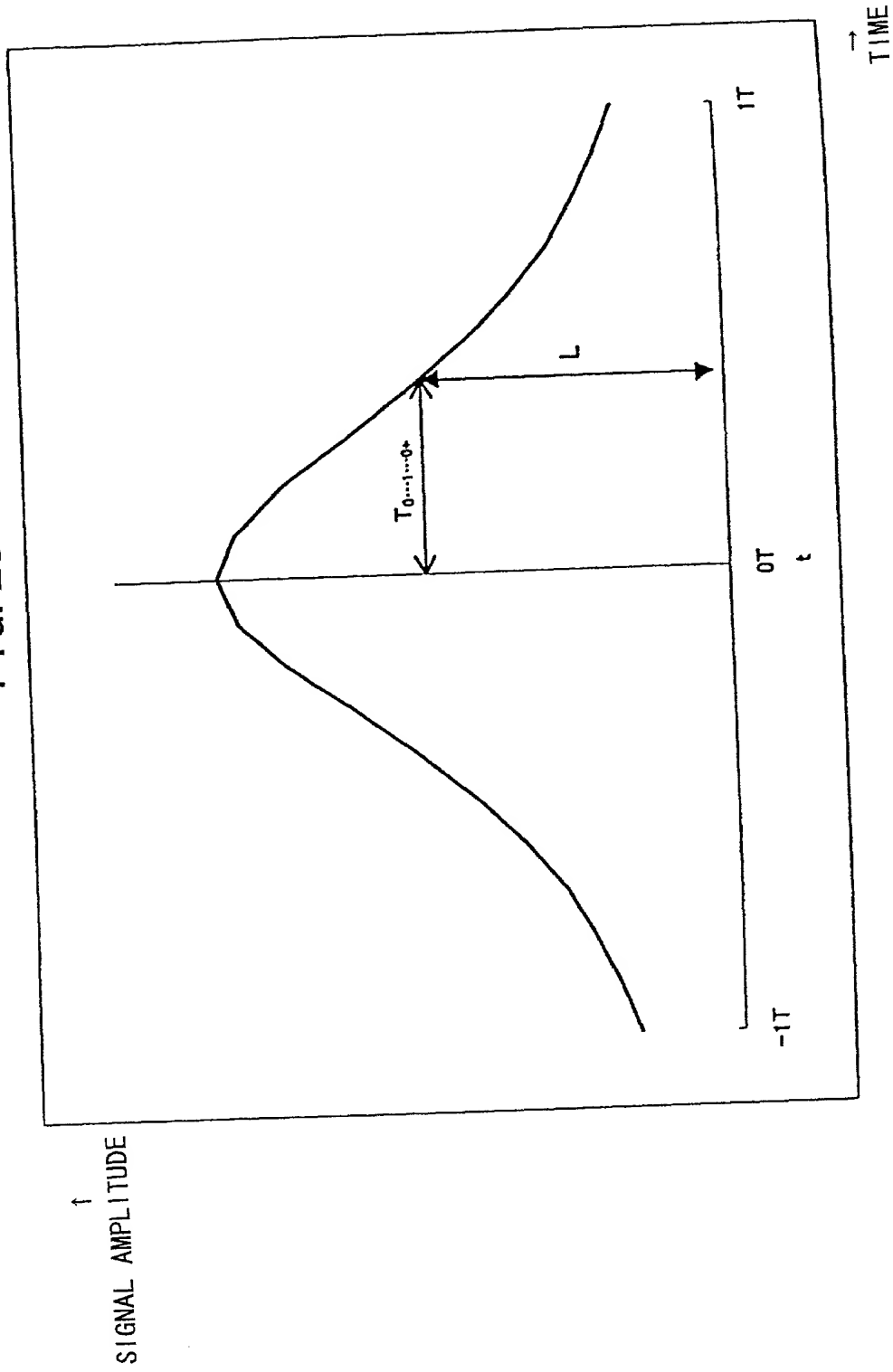


FIG.24

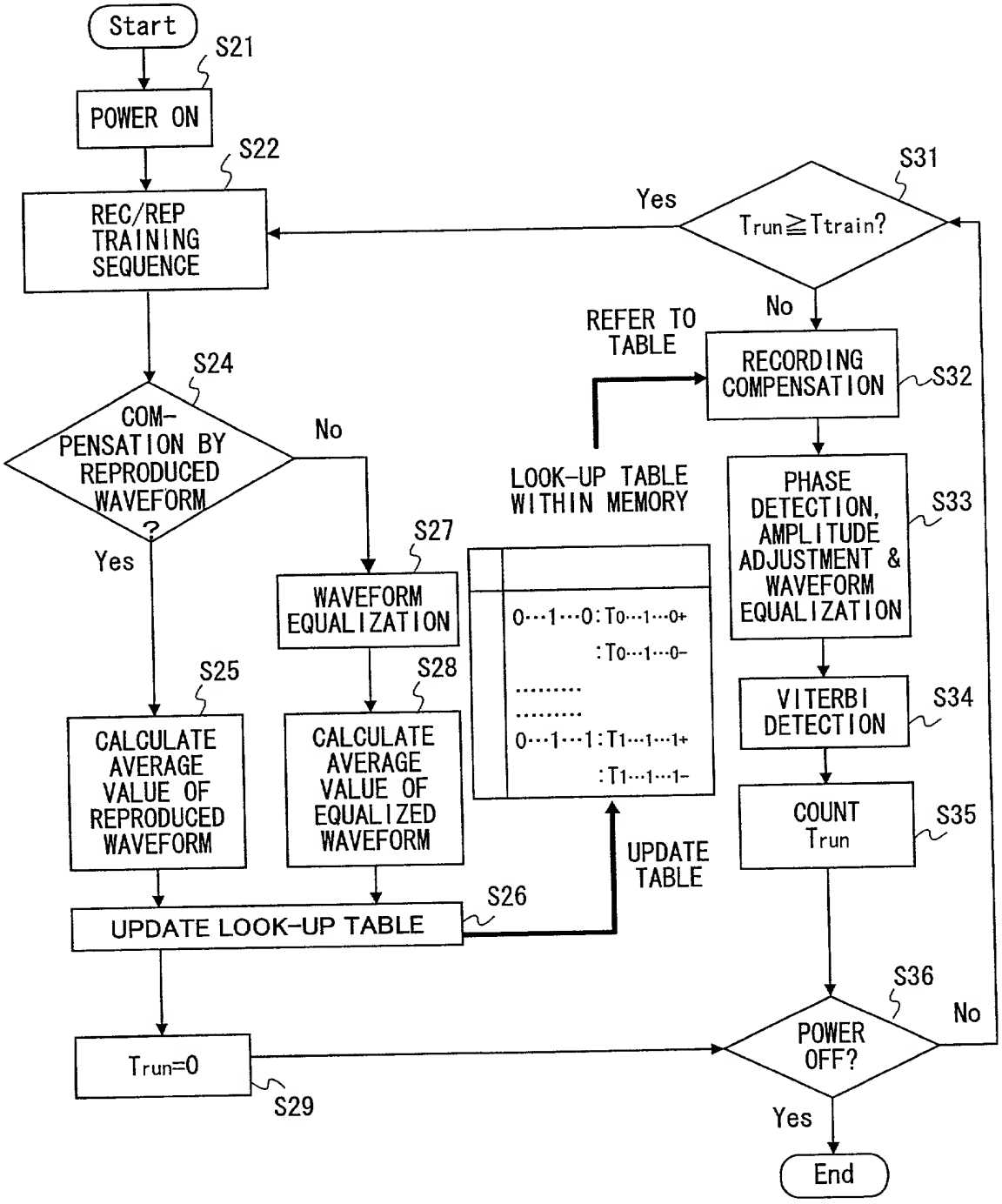
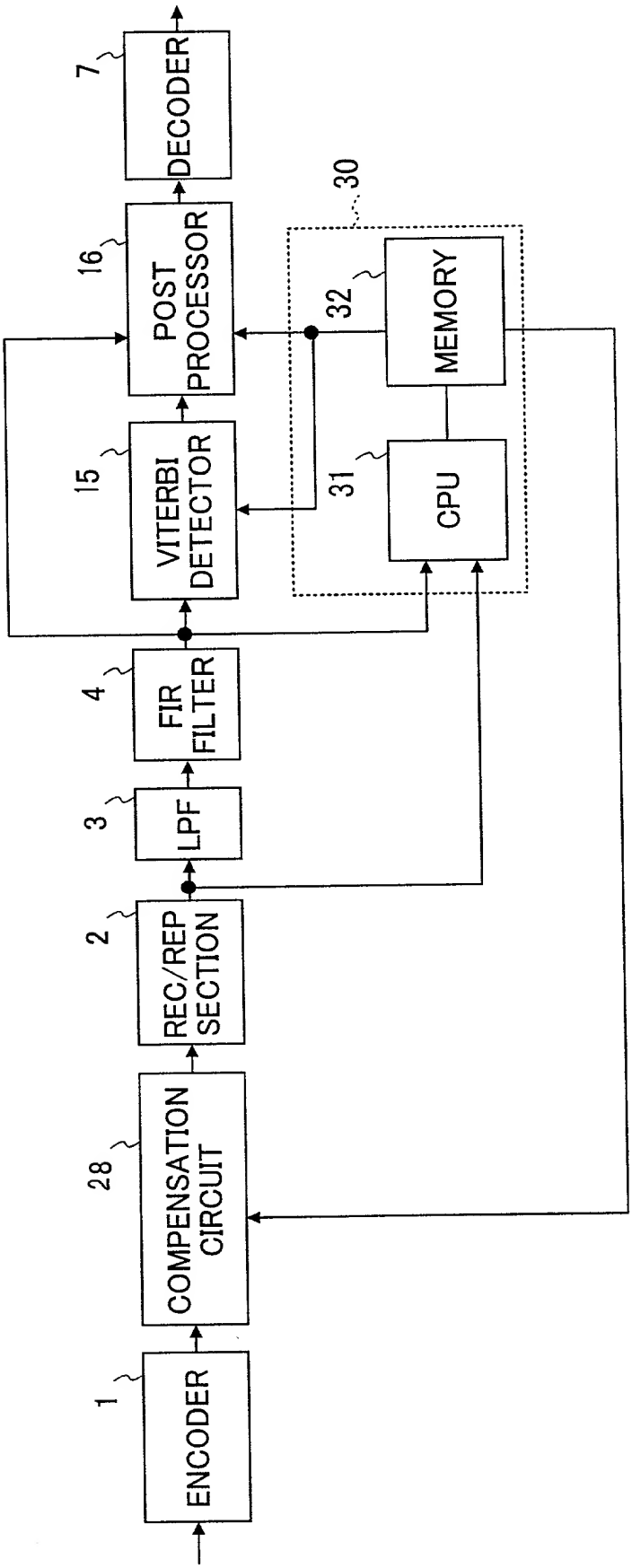

Start
S21
POWER ON
S22
REC/REP TRAINING SEQUENCE
S24
COM-PENSATION BY REPRODUCED WAVEFORM ?
Yes
No
S25
CALCULATE AVERAGE VALUE OF REPRODUCED WAVEFORM
S27
WAVEFORM EQUALIZATION
S28
CALCULATE AVERAGE VALUE OF EQUALIZED WAVEFORM
S26
UPDATE LOOK-UP TABLE
Trun=0
S29
LOOK-UP TABLE WITHIN MEMORY
0···1···0: To···1···0+
: To···1···0-
0···1···1: T1···1···1+
: T1···1···1-
UPDATE TABLE
REFER TO TABLE
S31
Trun≧Ttrain?
Yes
No
RECORDING COMPENSATION
S32
PHASE DETECTION, AMPLITUDE ADJUSTMENT & WAVEFORM EQUALIZATION
S33
VITERBI DETECTION
S34
COUNT Trun
S35
S36
POWER OFF?
No
Yes
End

FIG.25


ENCODER
1
COMPENSATION CIRCUIT
28
REC/REP SECTION
2
LPF
3
FIR FILTER
4
VITERBI DETECTOR
15
POST PROCESSOR
16
DECODER
7
30
MEMORY
32
CPU
31